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Box PATENT APPLICATION

Sir:

Transmitted herewith for filing is the patent  
application of:

Inventor(s): Helmut Horst TEWS and Jochen BEINTNER

For: NITROGEN IMPLANTATION USING A SHADOW EFFECT TO  
CONTROL GATE OXIDE THICKNESS IN DRAM SEMICONDUCTOR

This application includes:

12 pages: specification, claims and abstract  
2 sheets of drawings  
— photographs

Also enclosed is:

X Declaration and Power of Attorney  
— Information Disclosure Statement pursuant to 37 CFR 1.56.

The filing fee has been calculated as shown below:

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BASIC FEE	XXXXXXXX	XXXXXXXX	XXXXX \$710
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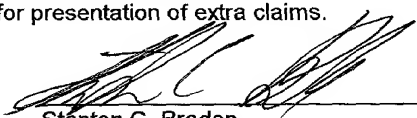
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APPLICATION FOR LETTERS PATENT  
OF THE UNITED STATES

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TITLE OF INVENTION: NITROGEN IMPLANTATION USING A  
SHADOW EFFECT TO CONTROL GATE  
OXIDE THICKNESS IN DRAM  
SEMICONDUCTOR

TO WHOM IT MAY CONCERN, THE FOLLOWING IS  
A SPECIFICATION OF THE AFORESAID INVENTION

09714356-11600

**NITROGEN IMPLANTATION USING A SHADOW EFFECT  
TO CONTROL GATE OXIDE THICKNESS IN  
DRAM SEMICONDUCTORS**

5

**BACKGROUND OF THE INVENTION**

1. Field of the Invention

10 The invention relates to fabrication of integrated circuit devices incorporating different thicknesses of gate oxides by using nitrogen implantation. Either angled nitrogen implantation or nitride spacers are used to create a "shadow effect", which limits the nitrogen dose close to the edges of the active area. This reduction of nitrogen does leads to an increased gate oxide  
15 thickness at the active area adjacent to the shallow trench and increases the threshold of the parasitic corner device and reduces sub  $V_t$ (threshold voltage) and junction leakage.

2. Description of The Related Art

20

In the arrangement of DRAM cell processing using a shallow trench isolation region to realize a small-size capacitor, gate oxide reliability of support oxides is limited by the thickness of the gate oxide at the AA (active area) corners. Therefore, careful optimization of the AA oxidation, (sacrificial) oxide,  
25 and gate oxidation is necessary to create the required AA corner rounding and the oxide thickness at the AA corner. In fact, in all too many instances, the oxide is thinner at the corners than at the AA area.

U.S. Patent 5,330,920 discloses a method of controlling gate oxide thickness in the fabrication of semiconductor devices. The process comprises:

30

forming a sacrificial gate oxide layer on select locations of a semiconductor substrate surface;

5            implanting nitrogen ions into the select locations of the substrate through the sacrificial gate oxide layer;

             thermally annealing the substrate and sacrificial gate oxide layer to assist pile-up of the nitrogen ions at the semiconductor substrate surface;

             removing the sacrificial gate oxide layer; and

10           thermally forming a gate oxide layer on the silicon semiconductor substrate surface, wherein the select locations having nitrogen ion implanted will have a thinner gate oxide layer than a non-implanted region.

             Fabrication of an integrated device using nitrogen implantation is disclosed in U.S. Patent 6,037,639. The process comprises:

15           providing a channel region defined by a source and drain region of a semiconductor substrate having a gate structure comprising an isolating oxide layer positioned on the channel region and the polysilicon layer positioned on the oxide layer. More specifically, the process comprises forming the nitrogen implanted regions over the semiconductor substrate by implanting nitrogen  
20           atoms into those regions and growing spacers from exposed portions of the polysilicon layer. During the spacer growth, the spacer grows vertically as well as laterally extending under the polysilicon edges. Diffusion of nitrogen atoms to the substrate surface forms silicon nitride under the gate edges, which minimizes current leakages into the gate polysilicon.

25           U.S. Patent 5,920,779 disclose a process for differential gate oxide thickness by nitrogen implantation for mixed mode and embedded VLSI circuits comprising:

             providing a semiconductor substrate having a surface, the semiconductor substrate comprising a first region on which a plurality of first MOS devices are  
30           to be formed and a second region on which a plurality of second MOS devices are to be formed;

             masking the second region and providing a first concentration of a first dopant in the semiconductor substrate at the surface of the first region without doping the second region;

5 removing the mask over the second region;  
masking the first region and providing a second concentration of a second dopant in the semiconductor substrate at the surface of the second region without doping the first region, wherein the second concentration is different than the first concentration;

10 oxidizing the surface of the semiconductor substrate to grow a first thickness of oxide on the first region of the semiconductor substrate and to grow a second, different thickness of oxide on the second region in a single oxidizing process; and

forming first MOS devices on the first regions of the semiconductor substrate incorporating the first thickness of oxide and forming second MOS devices on the second region incorporating the second thickness of oxide;  
15 wherein the first and second dopants are both nitrogen and the first concentration is greater than the second concentration.

In general, a typical way to achieve two oxide thicknesses in one oxidation step is to make use of local nitrogen implantation to reduce the oxidation rate at the implanted sites.  
20

The use of local nitrogen implementation to achieve two oxidation thicknesses in one oxidation step consist of utilizing the process integration scheme of:

25 growing of the sacrificial oxide;  
implantation of dopants through the sacrificial oxide;  
employing a photoresist mask to pattern an integrated circuit that includes the first transistor having a first dielectric thickness and a second transistor having a second dielectric thickness;

30 implanting nitrogen ions to create dual gate oxide devices;  
stripping off the photoresist mask and the sacrificial oxide; and  
subjecting the gate to oxidation.

Due to the fact that, in many cases, the gate oxide reliability of support oxide is limited by the thickness of the gate oxide at the AA (active area)

5 corners, and careful optimization of AA oxidation, sac oxide, and gate oxidation  
is necessary to create the required AA corner rounding and the oxide thickness  
at the AA corner, there is a need to limit the dual gate nitrogen dose in the AA to  
the inner part of the gate area to provide increased gate oxide thickness at the  
active area corner and thereby increase the threshold of the parasitic corner  
10 device, reduce sub Vt(threshold voltage) and junction leakage.

### SUMMARY OF THE INVENTION

One object of the present invention is to provide a dual gate oxide  
process for high performance DRAM systems to limit the dual gate nitrogen dose  
15 in the AA adjacent the STI oxide by use of a "shadow effect".

Another object of the present invention is to provide a dual gate oxide  
process for high performance DRAM systems that limit the dual gate nitrogen  
dose in the AA to the inner part adjacent the STI oxide by use of a "shadow  
effect" by eliminating the use of vertical nitrogen ion implantation under non-  
20 channeling conditions.

A further object of the present invention is to provide a dual gate oxide  
process for high performance DRAM systems by utilizing either an angled  
nitrogen ion implantation or nitride deposition to limit the nitrogen dose in the AA  
to the inner part adjacent the STI oxide by creating a "shadow effect" from the  
25 STI oxide which serves to reduce the N<sub>2</sub> dose at the AA edge to create an  
increased gate oxide at the AA corner and thereby increase the threshold of the  
parasitic corner device, and reduce sub Vt (threshold voltage) and junction  
leakage.

These and other objects of the invention will become more apparent by  
30 reference to the Brief Description Of The Drawings and Detailed Description Of  
The Preferred Embodiment Of The Invention.

5

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a graph comparing thickness reduction factor versus level of nitrogen dosage by implantation for a 800°C dry oxidation in pure oxidation.

FIG. 2 is a diagram depicting nitrogen implantation at a non-vertical angle  $\alpha$  with respect to the wafer surface at the normal, in which the AA at the inner part adjacent the STI oxide is under a "shadow effect".

FIG. 3 is a depiction of an alternative integration scheme using a nitride deposition to create the "shadow effect" and in which the shadow is complete without the necessity to use angled nitrogen ion implantation to reduce the dual gate nitrogen dose adjacent the STI oxide.

15

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENT OF THE INVENTION

In general, the invention process scheme for providing angled nitrogen implantation into the gate area to create a "shadow effect" during implantation is accomplished by:

- providing an AA(etching, oxidation, fill, planarization, and a pad nitride strip);
- growing a sacrificial oxide on the substrate;
- providing masking steps for channel implants;
- affecting channel implants;
- affecting a first angled nitrogen implantation without resist mask to create a "shadow effect" from the STI oxide to reduce the  $N_2$  dose at the AA edge to provide increased thickness gate oxide at the AA corners;
- providing a masking step for nitrogen ion implantation; and
- affecting a second angled nitrogen implantation to create a "shadow effect" from the STI oxide to reduce the  $N_2$  dose at the AA edge to provide increased thickness gate oxide at the AA corners.

In particular, the process flow for fabricating a dynamic random access memory cell utilizing angled nitrogen implantation of the invention will entail:

- 5 1) a. forming the active area by the well-known process of  
forming over a substrate, a patterned hard mask layer  
exposing portions of the substrate so as to define an  
isolation region; ;
- 10 b. etching exposed regions of the substrate using the patterned hard  
mask layer to form an isolation trench in the isolation region;
- c. oxidizing the substrate to form a thermal oxide layer in the isolation  
trench;
- d. depositing an oxide layer over the thermal oxide layer  
to fill unfilled portions of the isolation trench;
- 15 e. removing the patterned hard mask;
- f. planarizing the substrate and forming a pad nitride  
strip;
- 2) forming a sacrificial gate oxide layer in the areas of  
the semiconductor substrate where the pad nitride has been stripped off;
- 20 3) affecting channel implants in selected areas using resist  
masks;
- 4) affecting a first low dose angled nitrogen implant  
without using an implant mask in a manner to limit the nitrogen dose in the active  
area to the inner part of the gate area so that the angled nitrogen dose in the  
25 "shadow part" of the active area is less than the amount of the nitrogen dose  
implanted in the remaining non-shadowed area (to affect the spatial thickness  
distribution of all exposed oxide areas);
- 5) affecting masking so that nitrogen ions ( $N_2^+$ ) to be  
implanted do not penetrate the masked region; and
- 30 6) affecting a second angled nitrogen ion implantation in a  
manner so as to limit the dual gate nitrogen dose in the active area to the inner  
part of the gate area so that the angled nitrogen dose in the "shadow part" of the  
active area is less than the amount of the nitrogen dose implanted in the  
remaining non-shadowed area.



5 In general, nitrogen ion implantation is known to be done vertically under non-channeling conditions in the prior art, where the goal of the nitrogen ion implantation is to create a thinner oxide in the implanted areas, thereby leading to two oxide thicknesses for the non-implanted area and the nitrogen implanted area.

10 Reference is now made to FIG. 1, which shows a graph of thickness reduction due to  $N_2$  implantation followed by a thermal oxidation in pure oxygen at a temperature of  $800^\circ\text{C}$ . The thickness reduction factor is defined as the ratio of the oxide thickness without nitrogen implant divided by the oxide thickness with nitrogen implant.

15 In the context of the invention process, reference is made to the schematic diagram of FIG. 2 which shows nitrogen ions  $N_2$  implanted under an angle  $\nu$  with respect to the normal surface of the AA 10 of the wafer surface 11. Two implantations are conducted under  $+\nu$  and under  $-\nu$ . The nitrogen dose in the shadow area of the AA is half the amount of nitrogen ion dose implanted in the remaining, non-shadowed area.

20 The length of the shadow area  $x$  is calculated according to the following formula:

$$\tan \nu = x/h$$

where  $h$  is the height of the STI oxide 12 over the AA surface. When  $h = 500\text{A}$  (+/-  $150\text{A}$ ) and  $\nu = 60$  degrees the maximum value for  $x = 866\text{A}$ . If an angle of 15 degrees is chosen,  $x = 130\text{A}$  (+/-  $40\text{A}$ ). The shadow length can be chosen over a long range. The goal for  $x$  is approximately 10% of the ground rule, e.g.  $100\text{A} - 170\text{A}$  in the existing microelectronic technologies.

30 To comprehend the effect of the nitrogen implantation on oxide thickness, thick and thin oxides within the framework of dual gate technology are discussed separately.

1) Thick oxide: In the dual gate process known in the art, the thick oxide is not exposed to a nitrogen implantation. The invention uses a low dose nitrogen implant for the thick oxide to modify and optimize its spatial thickness

5 distribution. The nitrogen dose is chosen to be  $5 \times 10^{13}$ – $1 \times 10^{14} \text{cm}^{-2}$ . For the case  $1 \times 10^{14} \text{cm}^{-2}$  and using  $800^\circ\text{C}$  oxidation, a reduction of the oxide thickness of approximately 20% is achieved in the non-shadow region of the gate. In the shadow regions where only  $5 \times 10^{13} \text{cm}^{-2}$  is implanted, the oxide thickness is reduced by only 10%.

10 2) Thin oxide: The nitrogen dose is chosen to be approximately  $4 \times 10^{14} \text{cm}^{-2}$ . This gives a reduction of 70% with respect to the non-implanted case, or 50% to the case of the  $1 \times 10^{14} \text{cm}^{-2}$  implanted thick oxide. The oxide at the STI oxide edges is 35% thicker than in the non-shadow region.

FIG. 3, shows an alternative embodiment of the invention process that  
15 provides a "shadow effect" or shadow area SA which is complete or fixed, thereby eliminating the need to utilize angled nitrogen ion implantation and yet, achieve benefits as though angled nitrogen implantation had been used.

In this alternative embodiment of the invention process, the integration scheme utilizes a nitride spacer deposition to provide the shadow effect. In this  
20 alternative embodiment, a nitride deposition ND such as that of silicon nitride is performed after the channel implantation steps. Thereafter, optionally, steam oxidation may be employed to convert the nitride layer into an oxide. Following conversion of the nitride layer into an oxide by steam oxidation, vertical  
implantation of nitrogen ions as shown by the two downwardly pointing arrows is  
25 employed. Since the "shadow effect" as shown by x results from the nitride deposition, vertical nitrogen ion implantation still results in less nitrogen ion implantation in the area adjacent the STI oxide 13 as shown by x, than in the active area AA of wafer surface 14.

In this alternative integration scheme of the process of the invention,  
30 since the "shadow effect" is complete by virtue of the nitride deposition, it is not necessary to use angled nitrogen ion implantation.

5 We claim:

1. In a process for forming dual gate oxides for use in high performance DRAM systems or logic circuits, the improvement comprising using a "shadow effect" to control gate oxide thickness at active area (AA) corners adjacent a shallow trench isolation (STI) region, comprising:

10

- I)
  - a. forming an active area by depositing over a semiconductor substrate, a patterned hard mask nitride layer exposing portions of said substrate so as to define an isolation region;
  - 15 b. etching exposed regions of said substrate using said patterned hard mask layer to form an isolation trench in the isolation region;
  - 20 c. oxidizing said substrate to form a thermal oxide layer in the isolation trench and the capacitor trench;
  - d. depositing an oxide layer over the thermal oxide layer to fill unfilled portions of the isolation trench;
  - 25 e. removing said patterned hard mask;
  - f. planarizing said substrate and forming a pad nitride strip;
- 30 II) forming a sacrificial gate oxide layer in the areas of the semiconductor substrate surface where the pad nitride has been stripped off;

- 5 III) affecting channel implants in selected areas using resist masks;
- IV) affecting a first low dose angled nitrogen implant without using an  
implant mask in a manner to limit the nitrogen dose in the active  
area to the inner part of the gate area so that the angled nitrogen  
10 dose in the "Shadow part" of the active area is less than the amount  
of the nitrogen dose implanted in the remaining non-shadowed  
area to cause spatial thickness distribution of all exposed oxide  
areas.
- 15 V) affecting masking so that nitrogen ions ( $N_2^+$ ) to be implanted do not  
penetrate the masked region; and
- VI) affecting a second nitrogen ion implantation by employing a  
"shadow effect" inducing means at a temperature sufficient to  
20 provide a lesser amount of nitrogen ion dosage in the inner part of  
the gate area so that the angled nitrogen in the "shadow part" part  
of the active area is less than the amount of nitrogen dose  
implanted in the remaining non-shadowed area.

25 2. The process of claim 1 wherein said "shadow effect"  
inducing means is by angled nitrogen ion implantation at an angle either greater  
or less than  $90^\circ$  with respect to the surface normal of said semiconductor or  
wafer substrate.

30 3. The process of claim 1 wherein said "shadow effect"  
inducing means in step VI is by nitride spacers followed by vertical or  $90^\circ$   
nitrogen ion implantation.

5           4. The process of claim 2 wherein said oxidation is  
performed at about 900°C under dry conditions .

          5. The process of claim 2 wherein said oxidation is  
performed at about 800°C under a combination of dry and wet oxidation  
10 conditions.

          6. The process of claim 3 wherein said oxidation is  
performed at about 900°C under dry conditions.

15           7. The process of claim 3 wherein said oxidation is  
performed at about 800°C under a combination of dry and wet oxidation  
conditions.

          8. The process of claim 3 wherein said nitride is silicon  
20 nitride.

          9. The process of claim 3 wherein between said nitride  
spacers and vertical nitrogen implantation, steam oxidation is employed to  
convert said nitride to an oxide.

### ABSTRACT

Process for forming dual gate oxides for DRAM systems by using a "shadow effect" to control gate oxide thickness at AA corners adjacent a STI region, comprising:

5 I) a. forming AA by depositing over a semiconductor substrate, a patterned nitride layer exposing portions of the substrate to define an isolation region and a capacitor region within the isolation region;

b. etching exposed regions of substrate using patterned nitride layer to form isolation trench in isolation region and capacitor trench in capacitor region within isolation region;

10 c. oxidizing the substrate to form a thermal oxide layer in the isolation trench and the capacitor trench;

d. depositing oxide layer over thermal oxide layer to fill unfilled portions of isolation trench and capacitor trench;

15 e. removing patterned nitride mask;

f. planarizing substrate and forming a pad nitride strip;

II) forming sacrificial gate oxide layer on select locations of semiconductor substrate surface;

20 III) selectively etching sacrificial oxidation layer by using patterned resist as mask for channel implants;

IV) affecting channel implants for doping;

V) affecting masking so that nitrogen ions ( $N_2^+$ ) to be implanted do not penetrate masked region; and

25 VI) causing nitrogen ion implantation by a "shadow effect" inducing means to provide lesser amounts of nitrogen ion dosage in inner part of active area adjacent the STI oxide than in remaining non-shadowed AA area, to provide increased thickness gate oxide at the AA corners.

▲ 800C dry

N2 Dose (cm <sup>-2</sup> )	Thickness reduction Factor
0.0E+00	1.0
~5.0E+13	~1.1
~3.6E+14	~1.74
~4.2E+14	~1.83

A cross-sectional diagram of a substrate 10. A trench 11 is formed in the substrate. A layer 12 is deposited on the bottom surface of the trench 11. The thickness of the layer 12 is denoted by  $h$ . The depth of the trench 11 is denoted by  $x$ . An incident ray  $N_2$  enters the trench at an angle  $\phi$  relative to the normal (indicated by a dashed vertical line).

FIG. 2

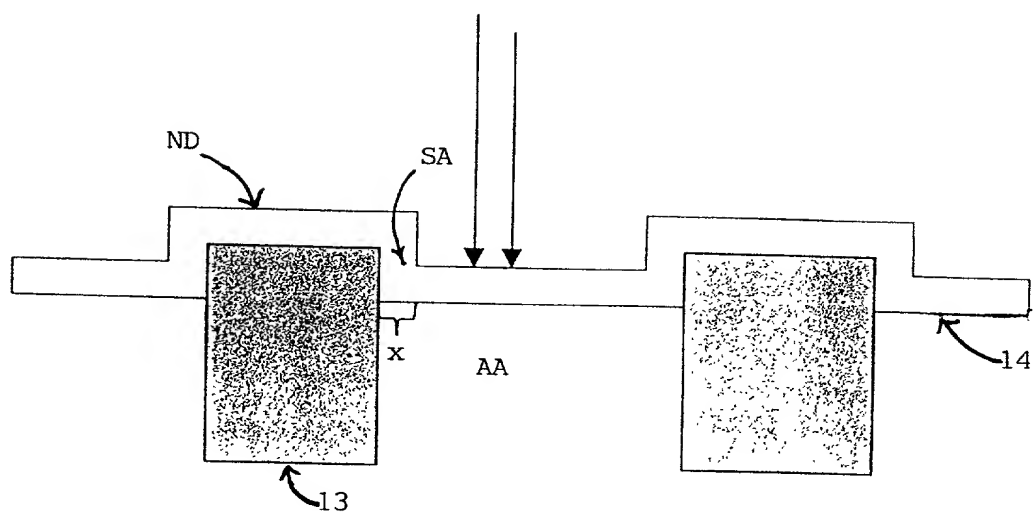


FIG. 3



**DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe we are the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**NITROGEN IMPLANTATION USING A SHADOW EFFECT TO  
CONTROL GATE OXIDE THICKNESS IN DRAM SEMICONDUCTOR**

the specification of which

x is attached hereto, and

\_\_\_\_\_ was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_

and was amended on \_\_\_\_\_ (if applicable)

Listing of named inventor(s): **Helmut Horst TEWS and Jochen BEINTNER**

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

**PRIOR FOREIGN APPLICATION(S)**

Priority claimed

(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No

I hereby claim the benefits under Title 35, United States Code, § 120 and/or 119 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)

009111" 9544250

Power of Attorney: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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